

92 學年度碩士班考試電子所計算機系統試題

1. Suppose there are 4 processes for execution. The process burst time, as well as the arrival time and priority of each process is indicated in the following table. Time is in milliseconds (ms).

| Process | Arrival Time | Burst Time | Priority |
|---------|--------------|------------|----------|
| P1 | 5 | 6 | 4 |
| P2 | 3 | 7 | 2 |
| P3 | 0 | 6 | 3 |
| P4 | 1 | 5 | 1 |

Draw the Gantt chart illustrating the scheduled execution of these processes and calculate the average waiting time for these processes using

- a) non-preemptive shortest job first scheduling algorithm
- b) Round Robin (quantum = 3ms)
- c) Preemptive priority (a smaller priority number implies a higher priority).

Note: CPU cannot stay idle if there are still unfinished processes. (18%)

2. In most systems, a process can allocate and de-allocate memory from its heap using malloc() and free(). Suppose the heap is managed with linked list. Each node in the list is either allocated or free. And the list kept sorted by address in increasing order. When malloc() is called, the list is searched for a free segment that is big enough (depending on the allocation algorithm), that segment is divided into an allocated segment (at the beginning) and a free segment. When free() is called, the corresponding segment should merge with its neighboring segments, if they are also free. Now suppose a process has a heap of 13KB, which is initially empty. During its execution, the process issues the following memory allocate/de-allocate calls (pi is just a pointer):

```

p1 = malloc(3KB);
p2 = malloc(4KB);
p3 = malloc(1KB); ← state 1
free(p2);          ← state 2
p4 = malloc(3KB);
free(p1);          ← state 3
p5 = malloc(2KB); ← state 4
    
```

Show what the heap is like after the above calls at state 1 state 2, state 3, and state 4, using

- a) first-fit,
- b) best-fit, and
- c) worst-fit algorithms respectively.

For simplicity, assume the memory begins at address 0, and ignore the memory used by the linked list itself. (18%)

3. Suppose a file system can have three disk allocation strategies, contiguous, linked and indexed. We have just read the information for a file from its parent directory. For contiguous and linked allocation, this gives the address of the first block; for indexed allocation this gives the address of the index block. Now we need to read the 20th data block into the memory. How many disk blocks do we have to read for each of the allocation strategies? (6%)

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4. When do page faults occur? Describe the actions taken by the operating system when a page fault occurs. (8%)
5. Explain the following terms: (20%)
 - a) RISC
 - b) Associative memory
 - c) MIMD computer
 - d) VLIW
6. Assume a processor currently has a clock rate of 400 MHz and takes 2 μ s to execute a program that has 250,000 instructions. (20%)
 - a) How many cycles does it take to execute this program?
 - b) What is the processor's CPI for this program?
 - c) What is the processor's MIPS rating for this program?

Assume that the processor's clock rate increases by 50 percent each year and that the architecture and machine organization of the processor do not change.

- d) How long in milliseconds does it take to execute this program after two years?
 - e) What is the processor's MIPS rating for this program after two years?
7. A basic microprogramming control unit is composed of the following units. Please briefly specify the functions of each unit and draw the basic architecture of microprogramming control unit using a block diagram. (10%)
 - CM: Control Memory
 - μ IR: Microinstruction Register
 - μ PC: Microprogram counter
 - DEC: Decoder
 - MUX: Multiplexer

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1. Fig. P1 shows a discrete enhancement MOSFET amplifier in which the input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. Please analyze this amplifier circuit to determine its small-signal voltage gain (v_o/v_i) and its input resistance. The transistor has threshold voltage $V_{tn}=1.5V$, transconductance parameters $k_n'(W/L)=0.25mA/V^2$, and channel length modulation parameter $\lambda=0.02V^{-1}$. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest. (25%)

2. Figs. P2(a) and P2(b) show a CMOS inverter and its voltage transfer characteristic. Find V_{OH} , V_{OL} , V_{IL} , V_{IH} , and evaluate the noise margins NM_H and NM_L . Assume the CMOS inverter is designed to have $V_{tn} = |V_{tp}| = V_t$ and $k_n'(W/L)_n = k_p'(W/L)_p$. (V_{tn} and V_{tp} are the threshold voltages of NMOS and PMOS; k_n' and k_p' are process transconductance parameters of NMOS and PMOS; $(W/L)_n$ and $(W/L)_p$ are aspect ratios of NMOS and PMOS, respectively.) (25%)

3. The equivalent circuit of the Colpitts oscillator is shown in Fig. P3. Please find the oscillation frequency and condition. (25%)

4. The 555 timer connected to implement an astable multivibrator is shown in Fig. P4. Please derive the period of the output voltage v_o . (25%)

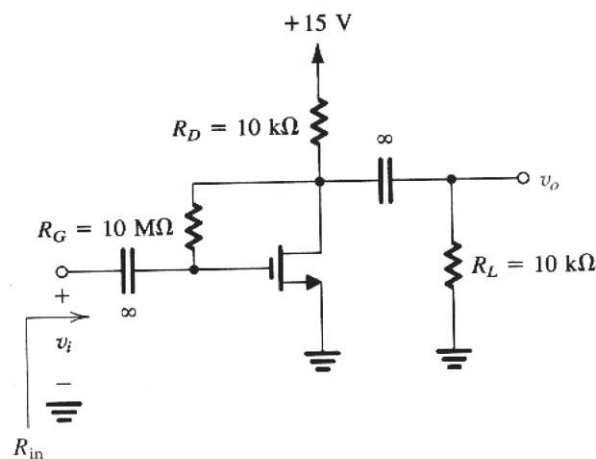


Fig. P1

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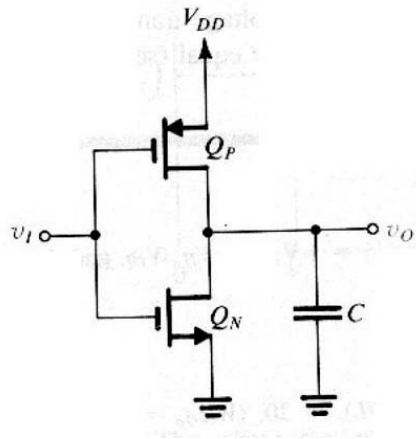


Fig.P2(a)

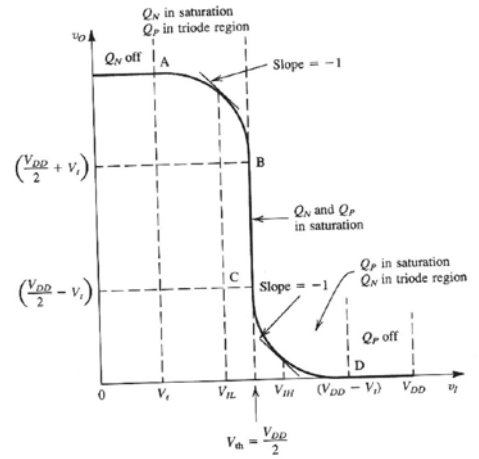


Fig. P2(b)

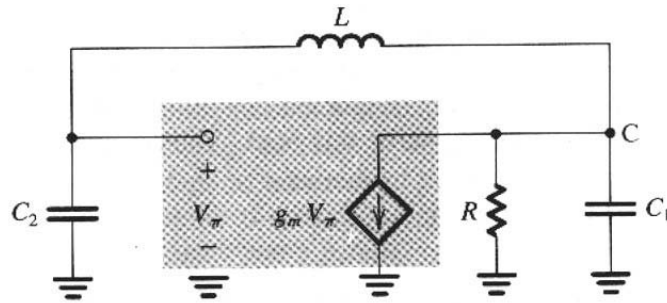


Fig. P3

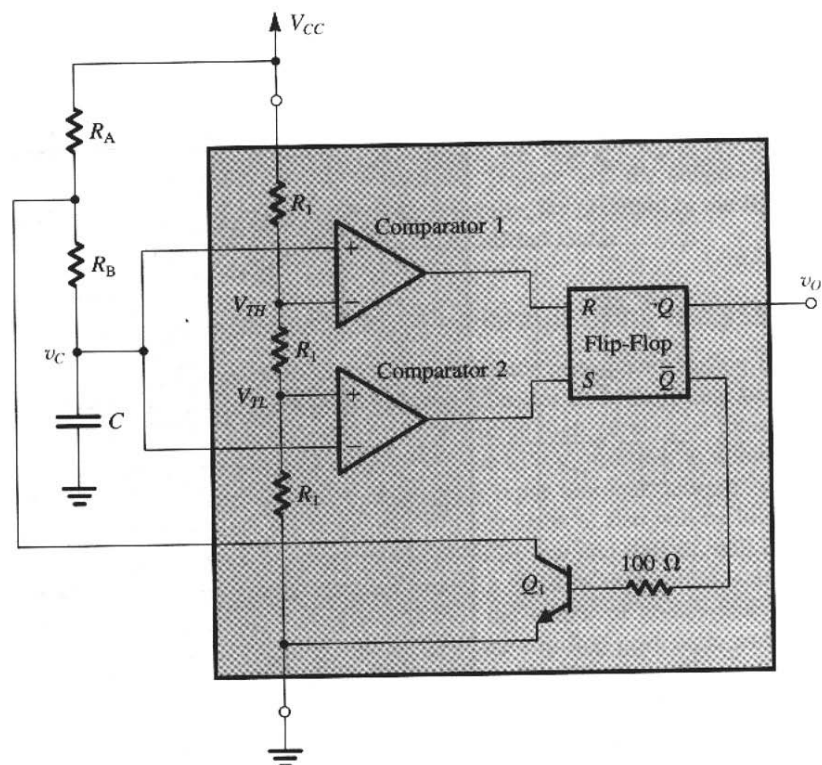


Fig. P4

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1. (a) Solve $x \frac{dy}{dx} + y = x^2 y^2$. (10%)
(b) Solve the initial-value problem $y'' + y = 4x + 10 \sin x$, $y(\pi) = 0$,
 $y'(\pi) = 2$. (10%)

2. (a) Evaluate $L \left\{ \int_0^t e^{\tau} \sin(t - \tau) d\tau \right\}$. (10%)
(b) Evaluate $L^{-1} \left\{ \frac{1}{(s^2 + k^2)^2} \right\}$. (10%)

3. Compute A^m for $A = \begin{bmatrix} 1 & 1 & -2 \\ -1 & 2 & 1 \\ 0 & 1 & -1 \end{bmatrix}$. (20%)

4. Find the frequency spectrum of the periodic square wave. The wave is the periodic extension of the function f : (20%)
$$f(x) = \begin{cases} 0, & -1/2 < x < -1/4 \\ 1, & -1/4 < x < 1/4 \\ 0, & 1/4 < x < 1/2 \end{cases}$$

5. (a) Evaluate $\oint_C \frac{2z + 6}{z^2 + 4} dz$, where the contour C is the circle $|z - i| = 2$. (10%)
(b) Evaluate $\oint_C \frac{e^z}{z^4 + 5z^3} dz$, where the contour C is the circle $|z| = 2$. (10%)